REMARKS/ARGUMENT

This is responsive to the Office Action dated September 17, 2002. A Petition for an extension of time is enclosed.

The Examiner objected to the drawings on the ground that the symbols referred to as "voltage sources" were objectionable. Enclosed are six drawing sheets containing proposed amendments in red. The voltage source symbols are being revised. In addition, in Fig. 2 the driver is being renumbered as "44" to correspond with the specification at page 2, line 21. In addition, obvious typographical errors are being corrected in Figs. 3, 4, and 6. The Examiner is requested to approve the proposed drawing corrections and withdraw the objection.

Claims 1-17 were rejected under 35 U.S.C. § 112, first paragraph, on the ground that the specification fails to adequately disclose the operation of the circuit. The Examiner alleged that the specification does not disclose "exactly what effect element 46 has on driver 44." The Examiner is referred to page 3, lines 10-21, which explains that when the output from comparator 46 goes high, the driver 44 is turned off. Therefore, this rejection under 35 U.S.C. § 112, first paragraph, is requested to be withdrawn.

Claims 1-17 were also rejected under 35 U.S.C. § 112, first paragraph, on the ground that the driver is deemed critical or essential to the practice of the invention, but is not included in the claims. Similarly, claims 1-17 were rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for reciting the control of power, without also reciting sufficient components for controlling power. The Applicants have responded to both of these rejections by appropriate amendments to include driving circuits in the independent claims. Therefore, these rejections are requested to be withdrawn.

The driving circuits are recited inferentially in claims 1, 9 and 17. New claims 18-20 depend respectively from claims 1, 9 and 17 and recite the driving circuits positively.

New claims 21 and 22 cover additional features of the invention.

Finally, claims 1-17 were rejected under 35 U.S.C. § 102(b) as being anticipated by Kimura et al. The rejection is respectively traversed. Each of claims 1, 9 and 17 recites, in combination with other features, "correction circuitry for preventing the sense input signal from including spurious information received . . . from the gating device." Examples of "spurious

information" in the present disclosure are high-frequency noise, page 3, lines 22-23; and a negative voltage spike, page 5, lines 7-10, which may appear on the sense input signal under certain circumstances.

The Examiner cited Fig. 1 in Kimura. The Examiner identified a power device 10, sensing circuitry 14 and 20, and a gating device 12 as corresponding to some of the features in the present claims. As for the claimed "correction circuitry," the Examiner merely stated that the "(remainder of the circuit), all connected and operating similarly as recited by Applicant" corresponded to the correction circuitry.

The rejection fails to set forth a *prima facie* basis for a rejection of these claims. Most fundamentally, the Examiner has not pointed out any portion of the reference which supports the rejection. 37 C.F.R. 1.104(b)(2), requires the Examiner to designate the particular part of the reference he is upon as nearly as practicable. The pertinence of the reference, if not apparent, must be clearly explained.

Second, the Kimura reference has been thoroughly reviewed and no "correction circuitry" for preventing, blocking, removing or any other processing of "spurious information received from the gating device" is seen. Even more particularly, the Examiner has not pointed to any disclosure of "spurious information" in the reference.

For both of these reasons, the rejection of claims 1-17 should be withdrawn.

It is further submitted that each of the dependent claims, in combination with its respective independent claim, recites patentable subject matter. It is unnecessary to quote each dependent claim in order to traverse the rejection, since none of the dependent claims have been mentioned in the Office Action.

In view of the foregoing amendments and remarks, allowance of claims 1-22 is requested.

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Asst. Commissioner for Patents, Washington, D.C. 20231, on January 17, 2003:

James A. Finder
Name of applicant, assignee or Registered Representative

Signature

January 17 2003
Date of Signature

JAF:msd

Respectfully submitted,

James A. Finder
Registration No.: 30,173
OSTROLENK, FABER, GERB & SOFFEN, LLP
1180 Avenue of the Americas
New York, New York 10036-8403
Telephone: (212) 382-0700

APPENDIX B

VERSION WITH MARKINGS TO SHOW CHANGES MADE
37 C.F.R. § 1.121(b)(iii) AND (c)(ii)

SPECIFICATION:

Paragraph at page 2, line 19:

In circuit 40, power FET 42, for example, represents either FET 12 or FET 14, with its gate connected either to the LO or the HO pin, which in turn receives gate control voltage from driver 44, representing either driver 22 or driver 30 on IC 20. Similarly, comparator 46 represents either comparator 24 or comparator 32, and buffer 48 represents either buffer 26 or buffer 34. Comparator 46 serves as part of sensing circuitry, providing a sense result signal in response to a sense input signal that includes information received at the DS/VF pin. The sense result signal at the output of comparator 46 includes information derived from the sense input signal about operation of FET 42.

Paragraph at page 5, line 17:

A central cause of the sensing problem is diode capacitance coupling during an off-to-on transition, leading to inaccurate VFB signal timing. As a result of coupling across diode 60, negative spikes and other spurious voltage variations can reach the DS/VF pin [as a result of] and cause inaccurately timed state changes by comparator 46. In addition, changes in the sizes of FET 42 and diode 60 as well as changes in the board and in the slope of segment 110 can affect VFB signal timing, contributing to VFB inaccuracies.

Paragraph at page 6, line 3:

Like the circuits described above, the new circuit includes sensing circuitry, which can include a comparator as described above or other appropriate components to provide a sense result signal in response to a sense input signal[:]. The sense input signal includes information received through a gating device, such as a diode or other appropriate device connected between the sensing circuitry and a power device; the sense result signal in turn includes information derived from the sense input signal about operation of the power device.

Paragraph at page 11, line 9:

During the off-to-on transition of FET 42, diode 60 remains temporarily off and therefore acts as a capacitor, so that a high frequency negative spike could pass through to the DS/VF pin. But segment 202 continues at the same voltage because an active impedance, provided either by element 162 in Fig. 4 or transistor 192 in Fig. 5, holds the voltage at the DS/VF pin and sinks high frequency spikes. As a result, the active impedance prevents the spikes from reaching the "+" input of comparator 46, and segment 204 continues at the same voltage because the output from comparator 46 is unchanged.

CLAIMS:

AMENDED 1. A power control circuit for controlling power provided across a power device by a driving circuit, comprising:

sensing circuitry for providing a sense result signal for controlling said driving circuit in response to a sense input signal, the sense input signal including information received through a gating device connected between the sensing circuitry and the power device; the sense result signal including information derived from the sense input signal about operation of the power device; and

correction circuitry for preventing the sense input signal from including spurious information received from the gating device.

AMENDED 9. An integrated power control circuit for controlling power provided across a power device by a driving circuit, comprising:

a sensing node for connecting to the power device through a gating device;

sensing circuitry for providing a sense result signal for controlling said driving circuit in response to a sense input signal, the sense input signal including information received at the sensing node through the gating device; the sense result signal including information derived from the sense input signal about operation of the power device; and

correction circuitry for preventing the sense input signal from including spurious information received at the sensing node from the gating device.

AMENDED 17. An integrated power control circuit for controlling power by respective high side and low side driving circuits across high and low side power devices connected in a half bridge, the circuit comprising high side circuitry for controlling the high side power device and low side circuitry for controlling the low side power device;

the high side circuitry comprising:

a first sensing node for connecting to the high side power device through a first gating device;

first sensing circuitry for providing a first sense result signal for controlling said high side driving circuit in response to a first sense input signal, the first sense input signal including information received at the first sensing node through the first gating device; the first sense result signal including information derived from the first sense input signal about operation of the first power device; and

first correction circuitry for preventing the first sense input signal from including spurious information received at the first sensing node from the first gating device; and

the low side circuitry comprising:

a second sensing node for connecting to the low side power device through a second gating device;

second sensing circuitry for providing a second sense result signal for controlling said low side driving circuit in response to a second sense input signal, the second sense input signal including information received at the second sensing node through the second gating device; the second sense result signal including information derived from the second sense input signal about operation of the second power device; and

second correction circuitry for preventing the second sense input signal from including spurious information received at the second sensing node from the second gating device.